Fabrication and Characterization of bulk FinFETs for Future Nano-Scale CMOS Technology

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- Simulation Study
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  - by Spacer Technology
  - by Selective Si_3N_4 Recess
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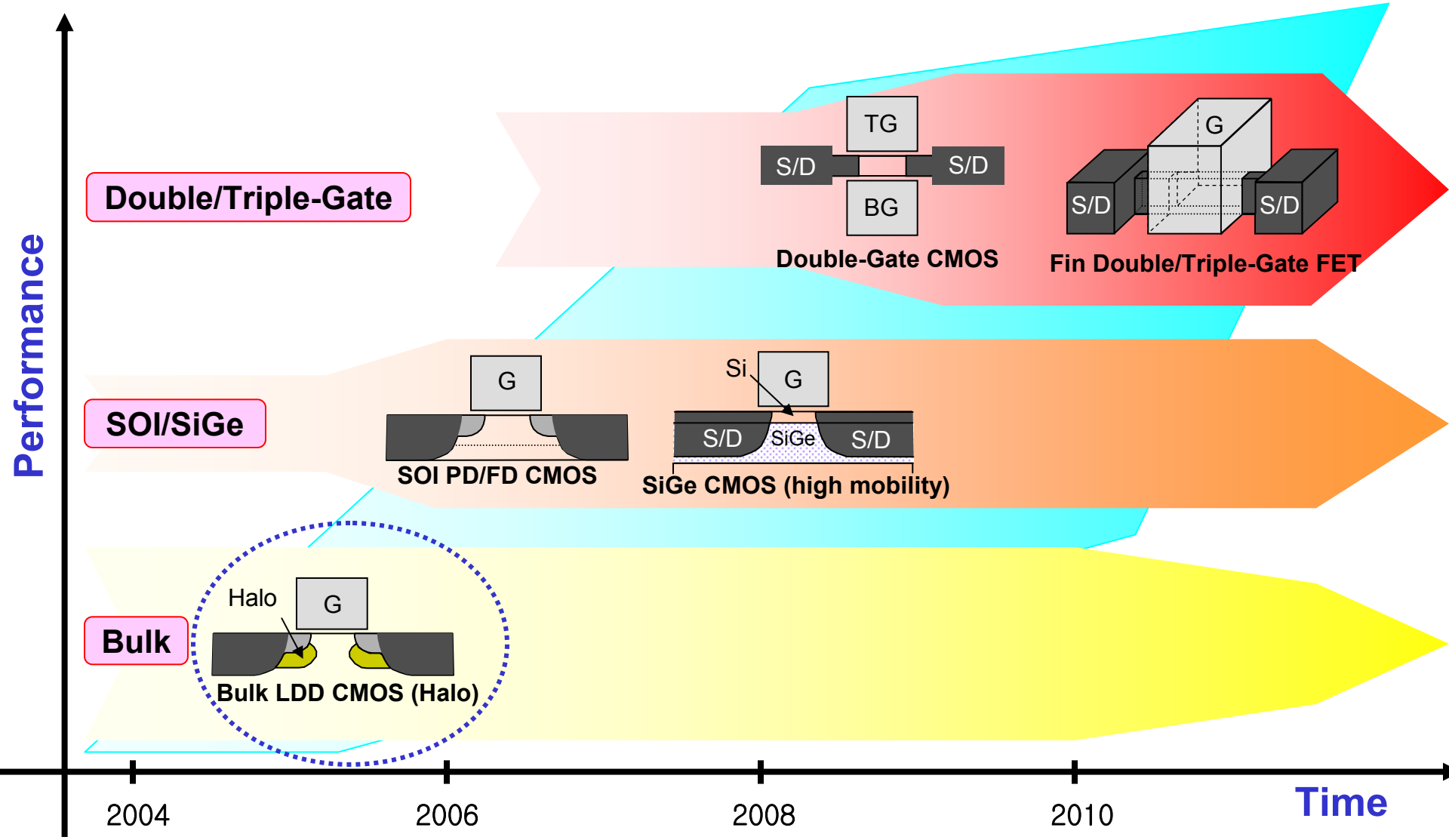
Introduction: Technology Roadmap Beyond Bulk LDD CMOS

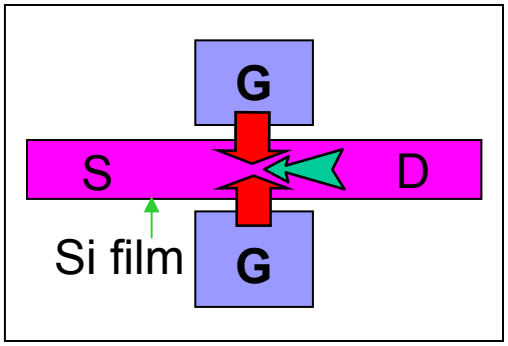


Introduction

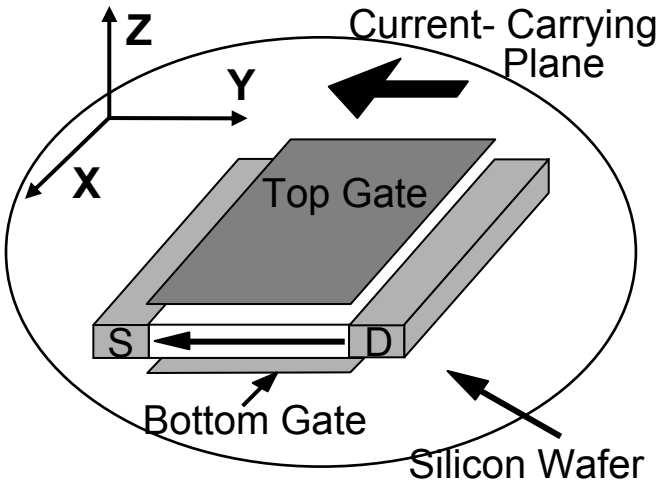
- **Driving Force of CMOS Scaling-down:**
  → **High Performance and High Integration Density**

- **A Promising Device Structure**
  → **Double/Triple-Gate MOSFETs (or FinFETs)**

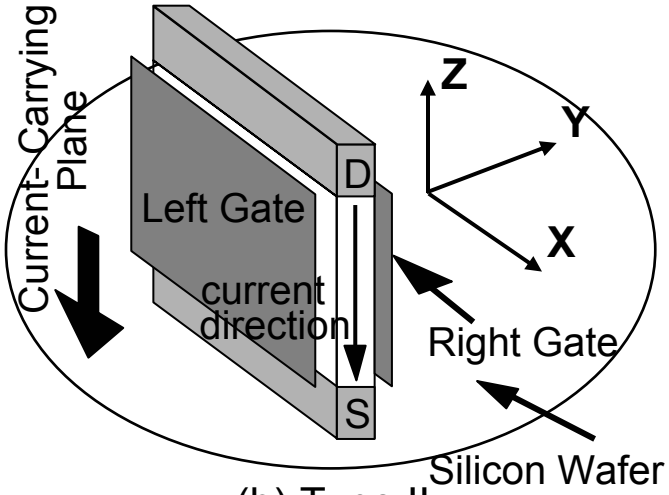
- **Why Double/Triple-Gate Transistor?**
  → **Robustness against SCE**
  → **Higher Current Drivability**
  → **Good Subthreshold Swing**



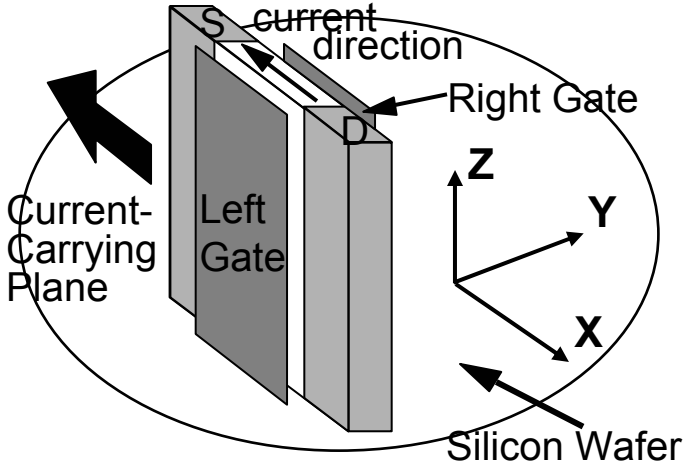
Introduction: Types of Double-Gate Transistors



(a) Type I



(b) Type II



(c) Type III

Process technology of FinFET is easy and compatible with conventional fabrication process

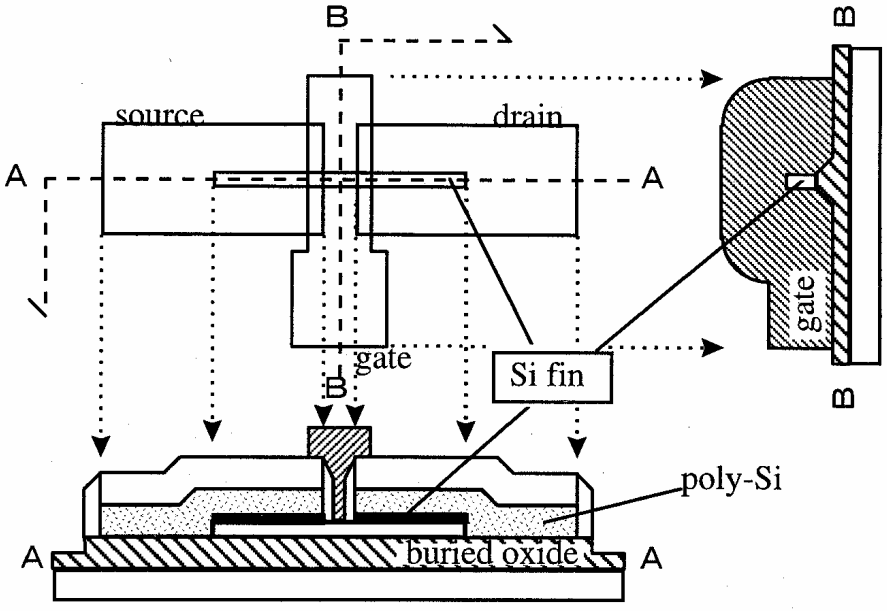
H. P. Wong et al., IBM, vol. 87, no. 4, p.537, 1999, Proceedings of the IEEE

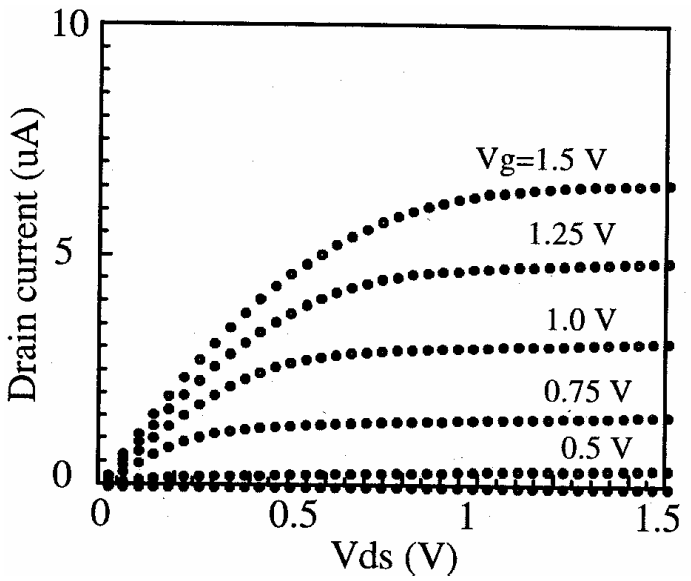
Types of Double/Triple-Gate Transistors

Type / Key Geometry	Type I (Planar DG FETs)	Type II (Vertical DG FETs)	Type III (FinFETs)	(Triple-Gate MOSFETs)
Gate Position	Top/Bottom	Left/Right (or Cylinder)	Left/Right	Left/Right/Top
Body Shape	Horizontal	Vertical	Vertical	Vertical
Current Carrying Plane	Horizontal Surfaces	Side Surfaces	Side Surfaces	Side Surfaces
Current Flow Direction	Horizontal	Vertical	Horizontal	Horizontal

Double-Gate Transistor (SOI FinFET)

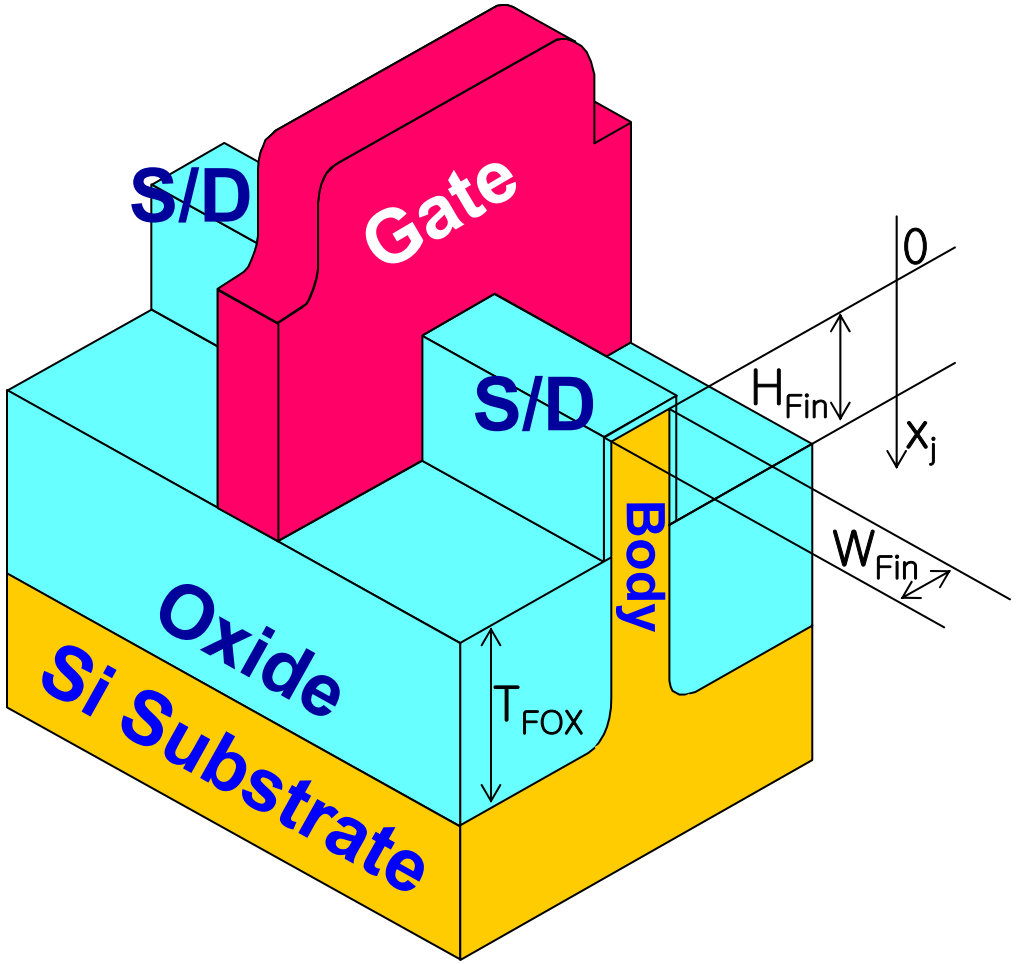
- **FinFET**
  - simple, self-aligned double-gates
  - good process compatibility
  - thickness control of fin body
  - RIE damage on the channel, high S/D resistance





* D. Hisamoto et al., UC Berkeley, p.1032, IEDM 1998

Body-Tied Double/Triple-Gate MOSFET Using Bulk Wafer (Bulk FinFET)



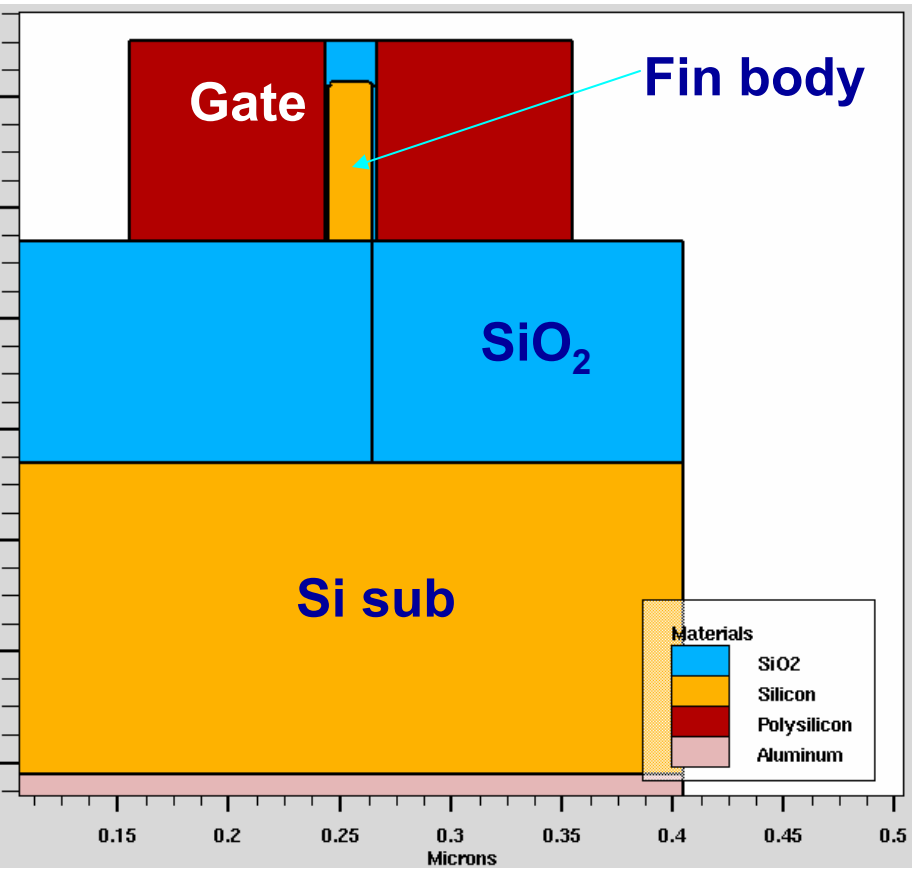
Schematic 3-D View

- Low wafer cost
- Low defect density
- Less back-bias effect
- High heat transfer rate to substrate
- Good process compatibility

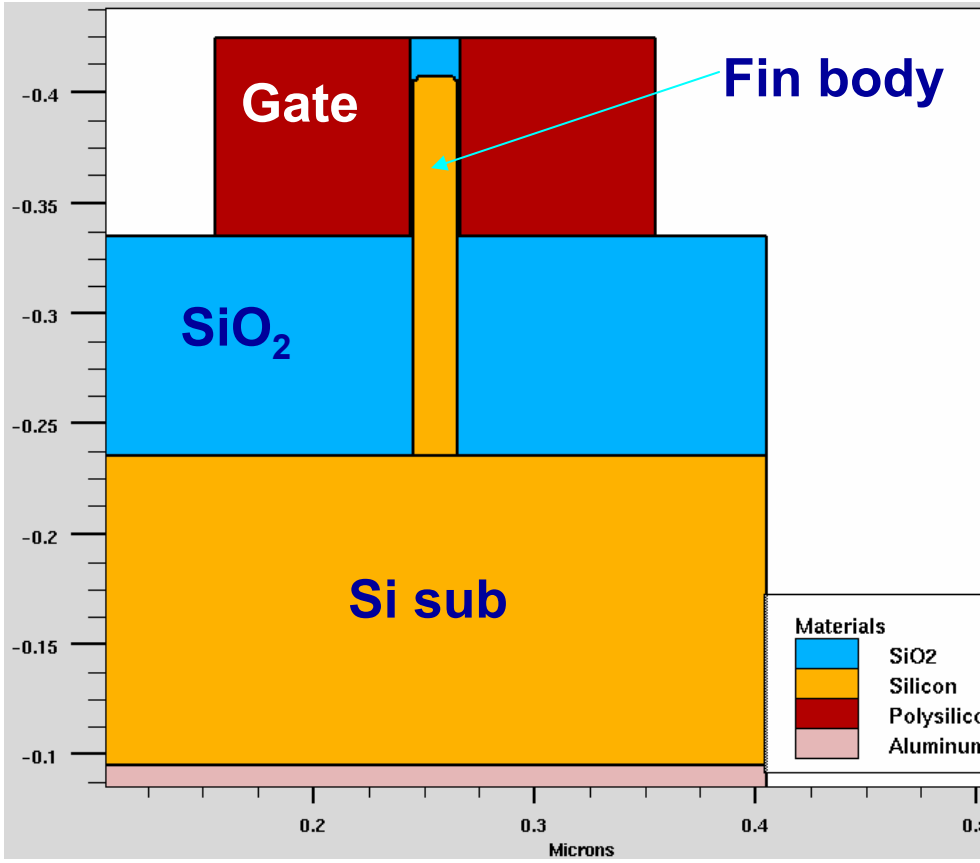
World 1st Cost-Effective Double/Triple-Gate MOSFETs

* J.-H. Lee., Korea/Japan/USA patent

Cross-Sectional Views (Body Structure) for 3-Dimensional Device Simulation

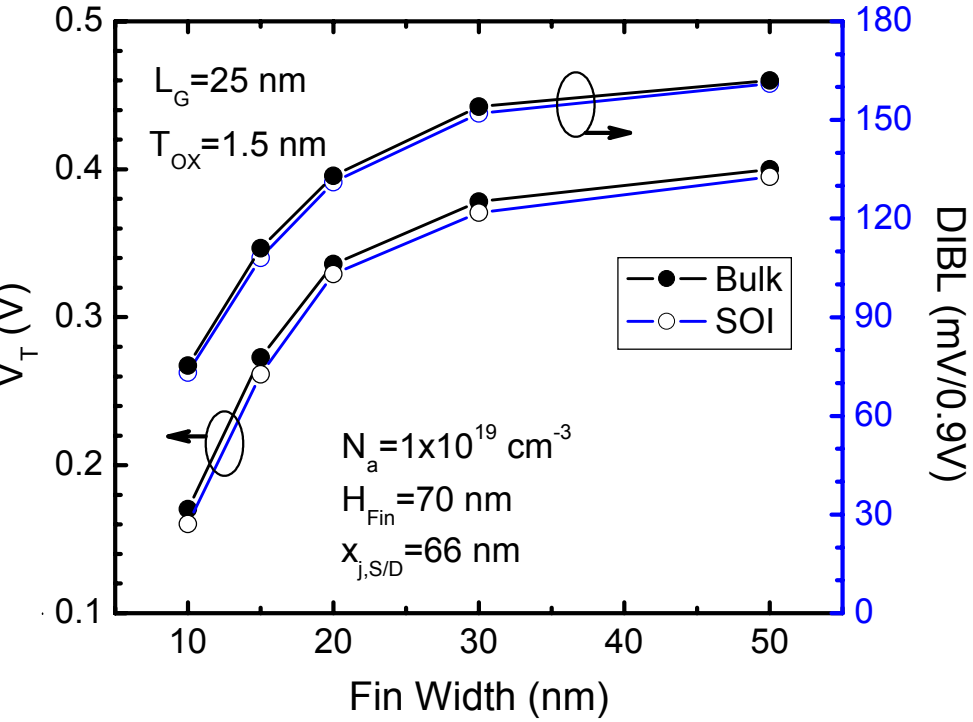


SOI FinFET

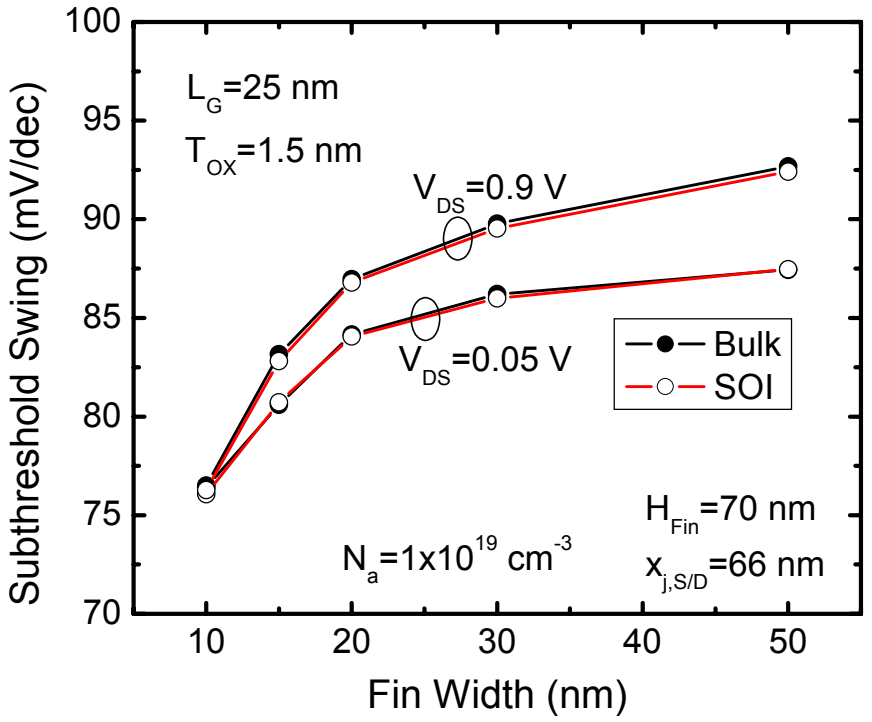


Bulk FinFET

3-D Simulation Results



V_T and DIBL versus Fin Width

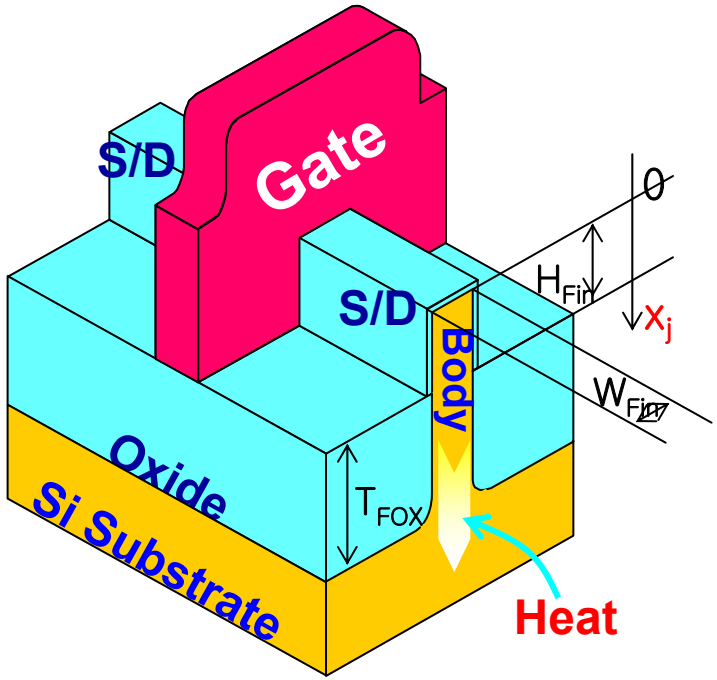


Subthreshold Swing versus Fin Width

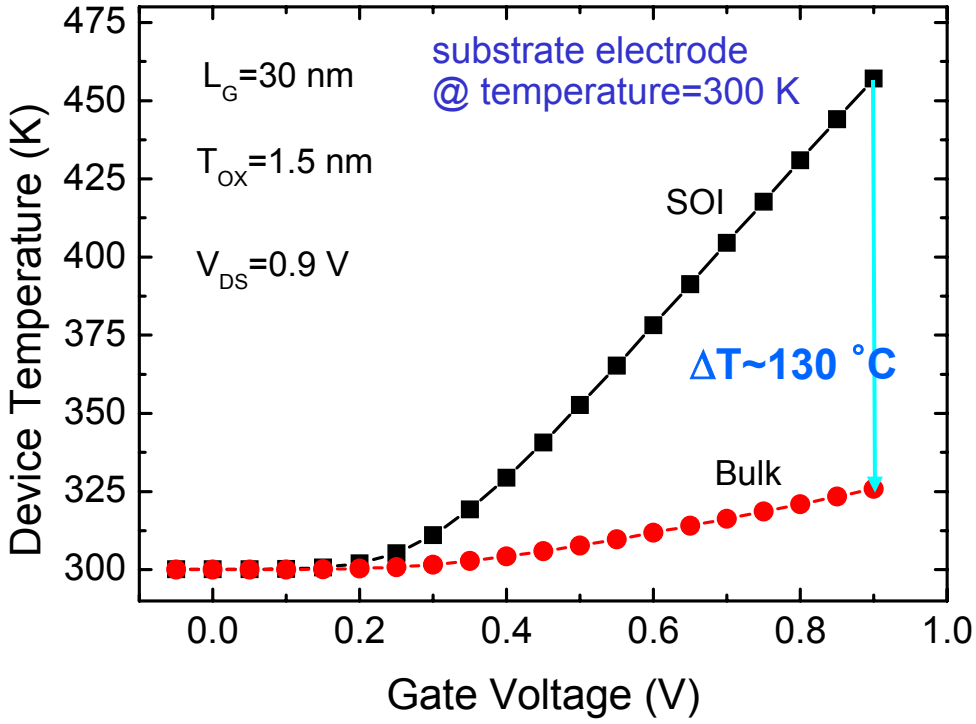
$$V_T = \Phi_{MS} + 2\phi_B + \frac{qN_{sub}t_b}{2C_{ox}}$$ for fully depleted body

* J.-H. Lee et al., KNU, p. 102, Si Nanoelectronics Workshop 2003

3-D Simulation Results



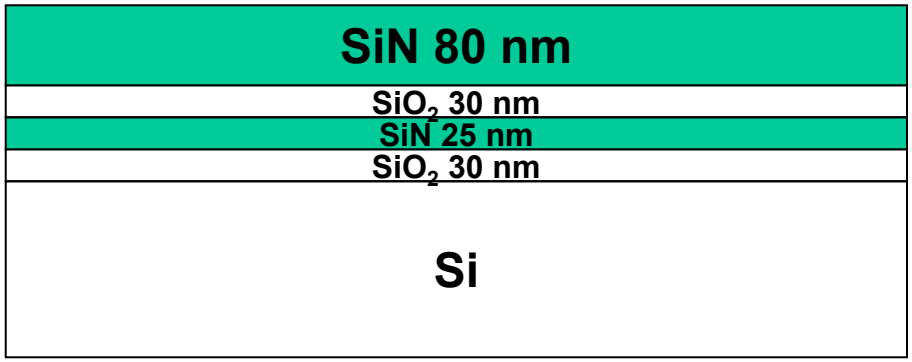
3-D Schematic View of Heat Transfer from Body to Substrate



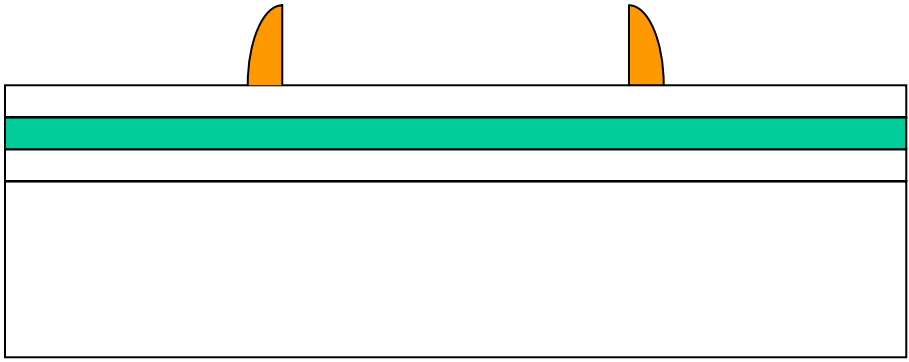
Device Temperature versus Gate Voltage

J.-H. Lee et al., KNU, p. 102, Si Nanoelectronics Workshop 2003

Fabrication Steps by Using Spacer Technology



4 Stack Layer Growth and Deposition



SiN Removal Using Phosphoric Acid

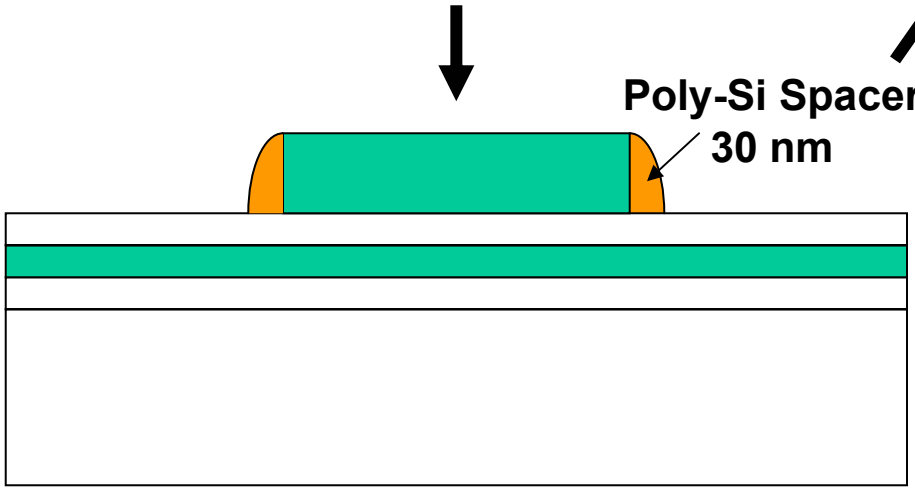
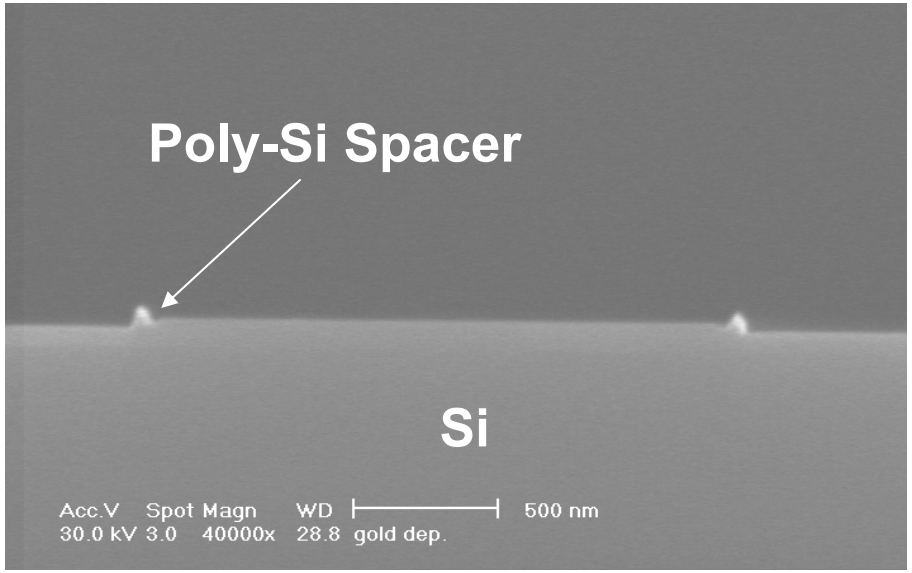
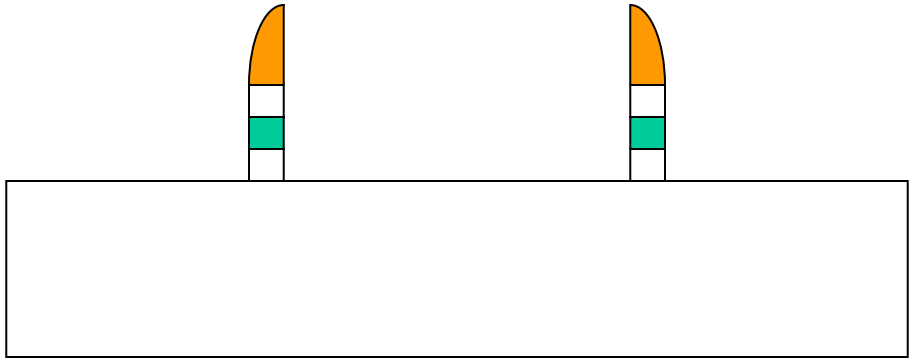


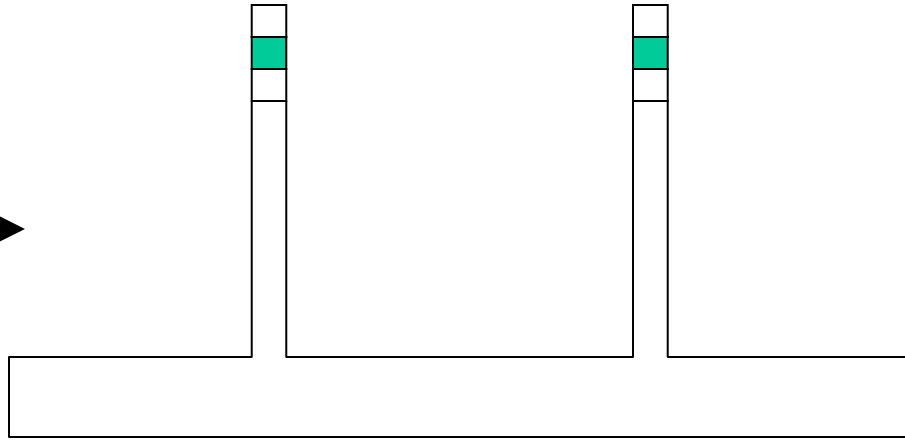
Photo Lithography, SiN Etching,
Poly-Si Depo., and Dry Etching



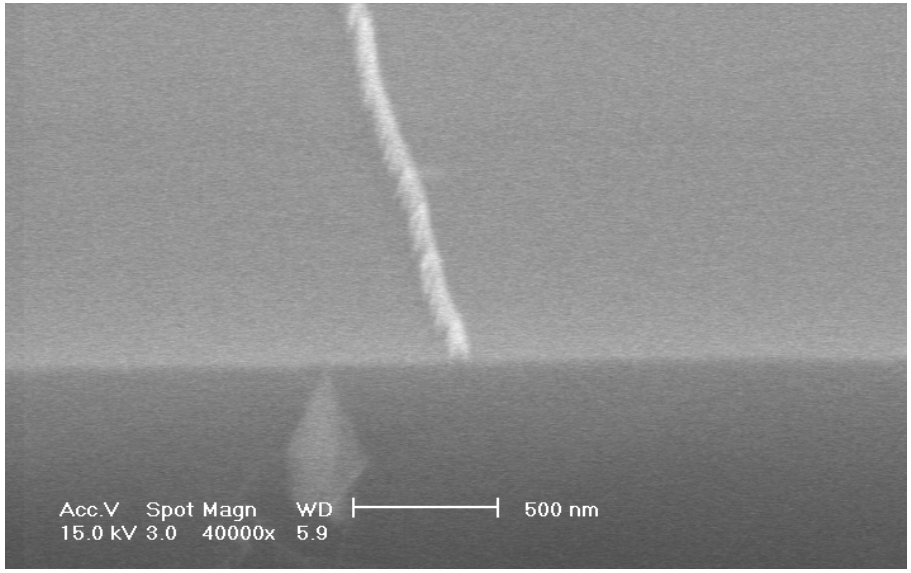
Fabrication Steps

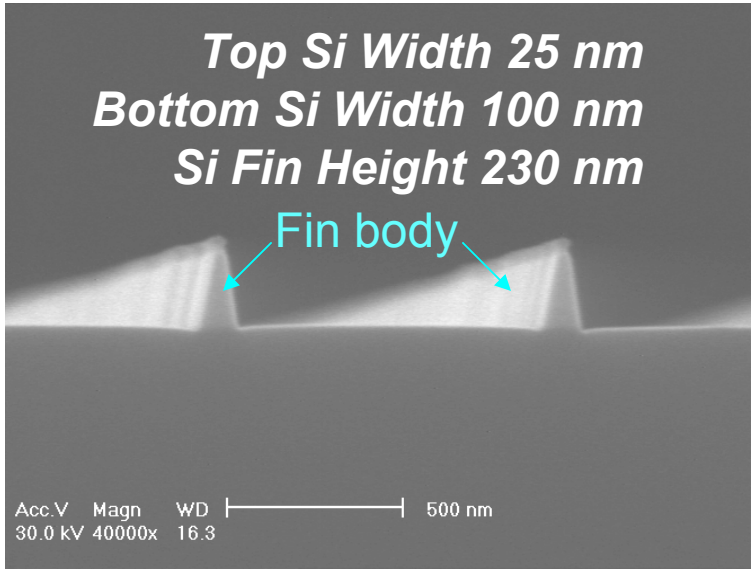


SiO_2, SiN, and SiO_2 Dry Etching

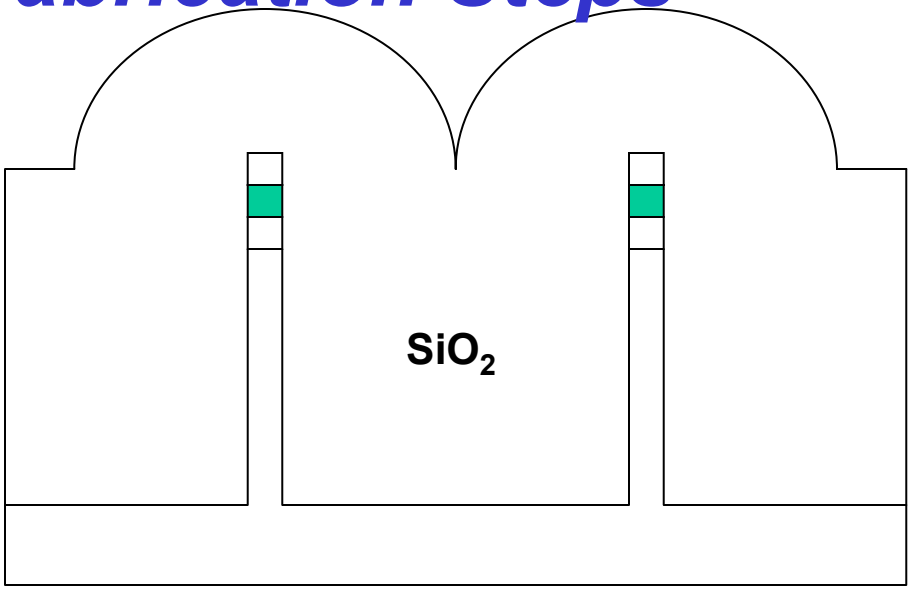


Fin Dry Etching

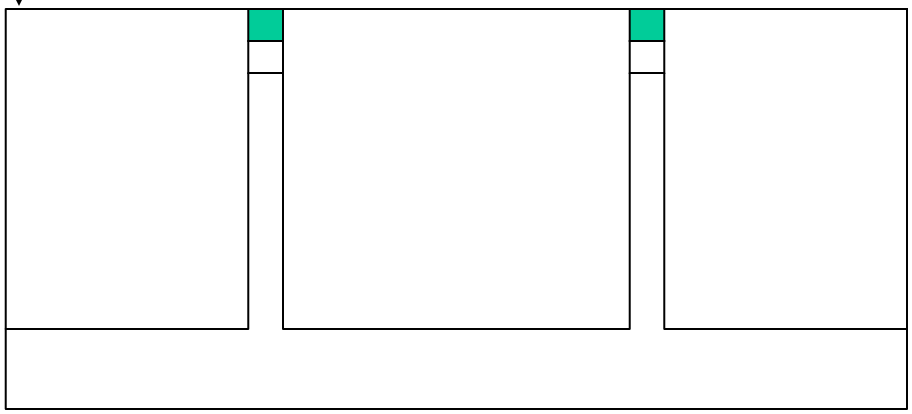




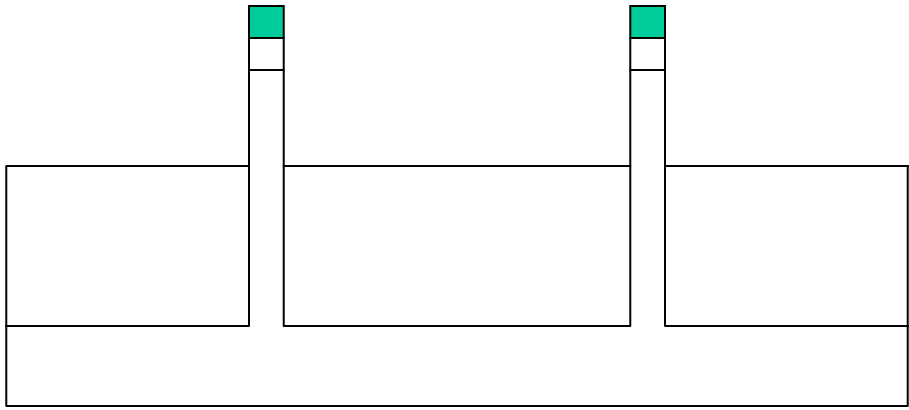
Fabrication Steps



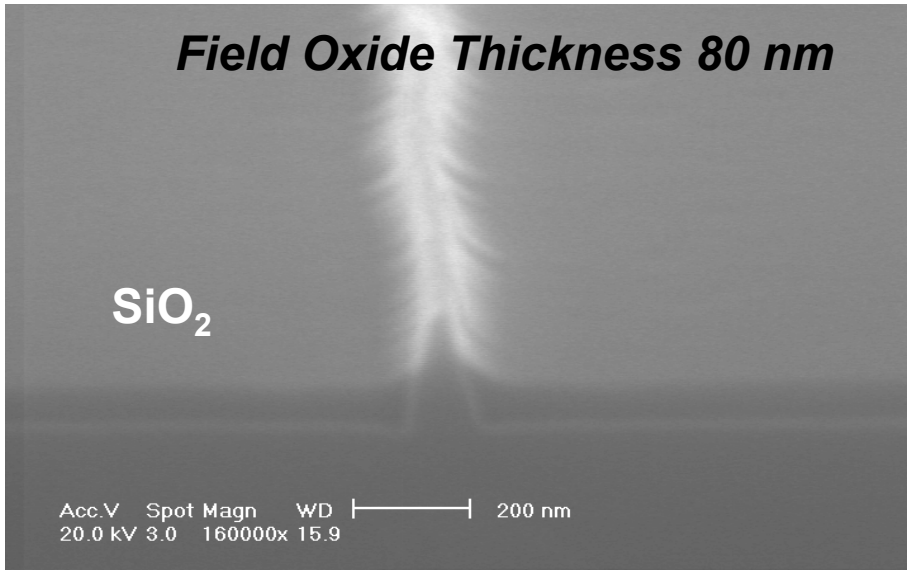
Thin Ox., Filling, and Densification



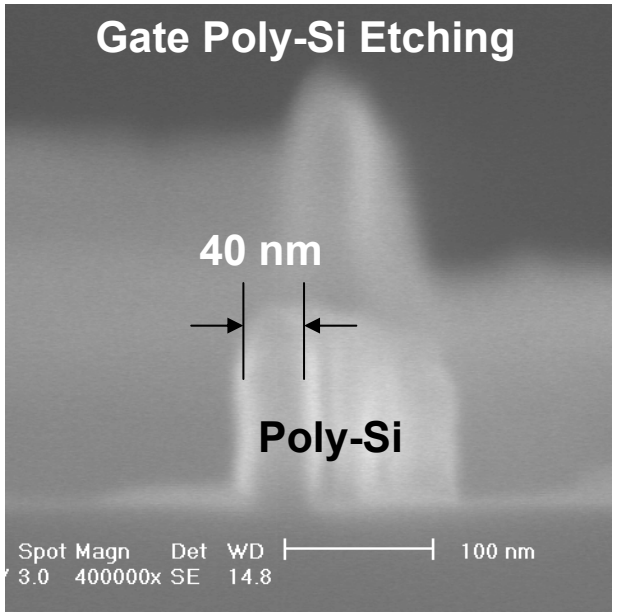
Chemical Mechanical Polishing (CMP)

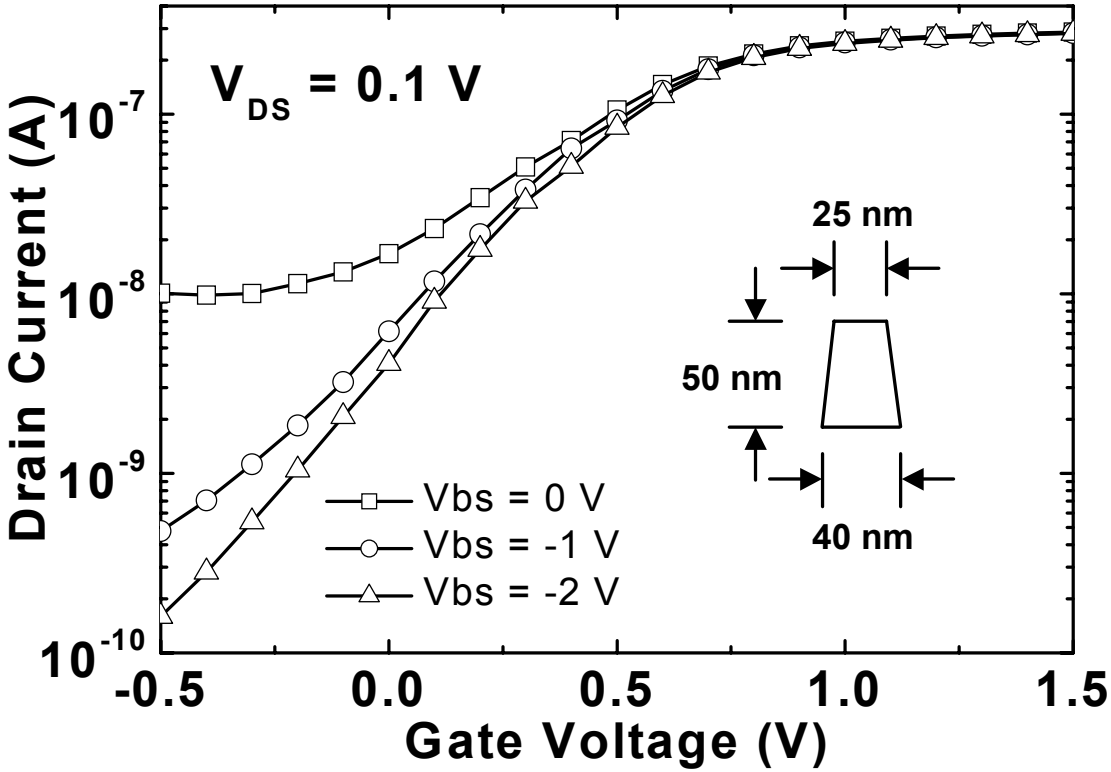


Wet Etch-back



First Body-Tied Triple-Gate MOFET (Bulk FinFET)

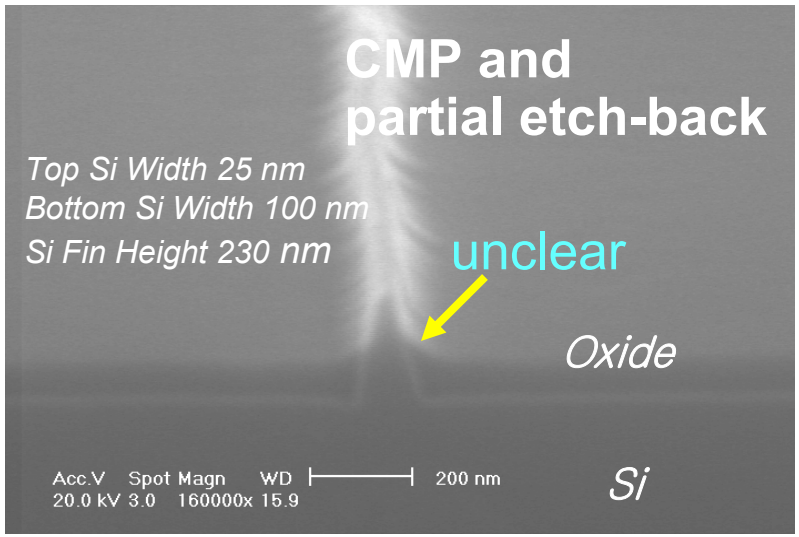


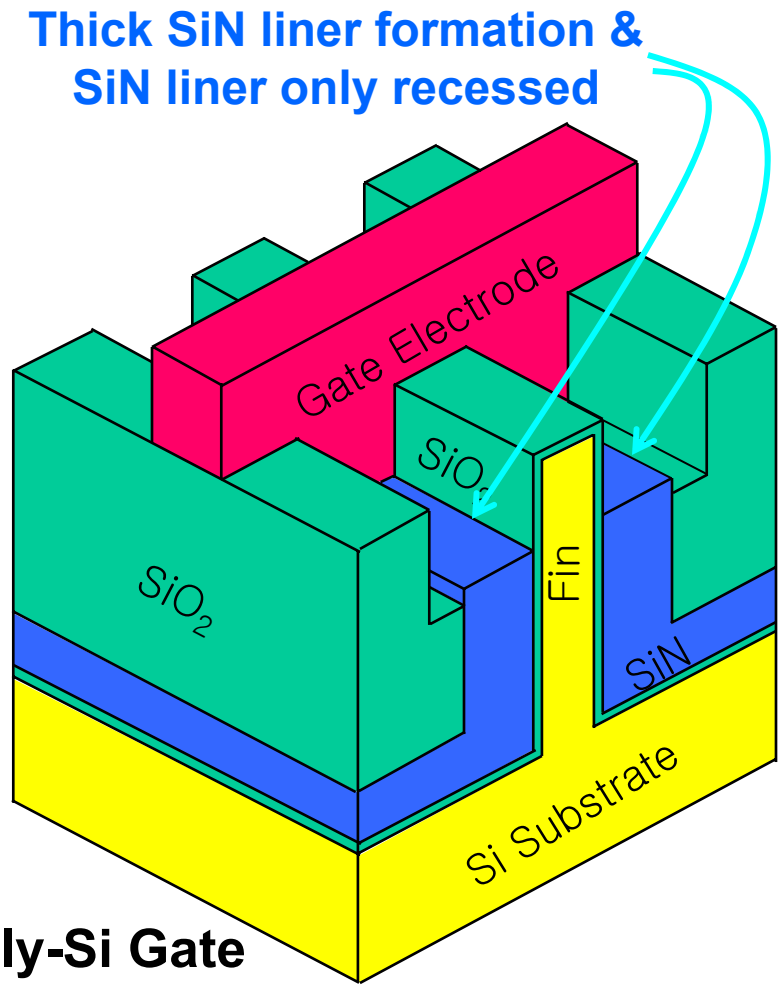


I_D-V_{GS} Characteristics of 40 nm bulk NFiNFET

* T. Park et al., SNU/KNU, Nanomes03 2003
* T. Park et al., SNU/KNU, Physica E19, p.6, 2003

Modified Structure of Bulk FinFET

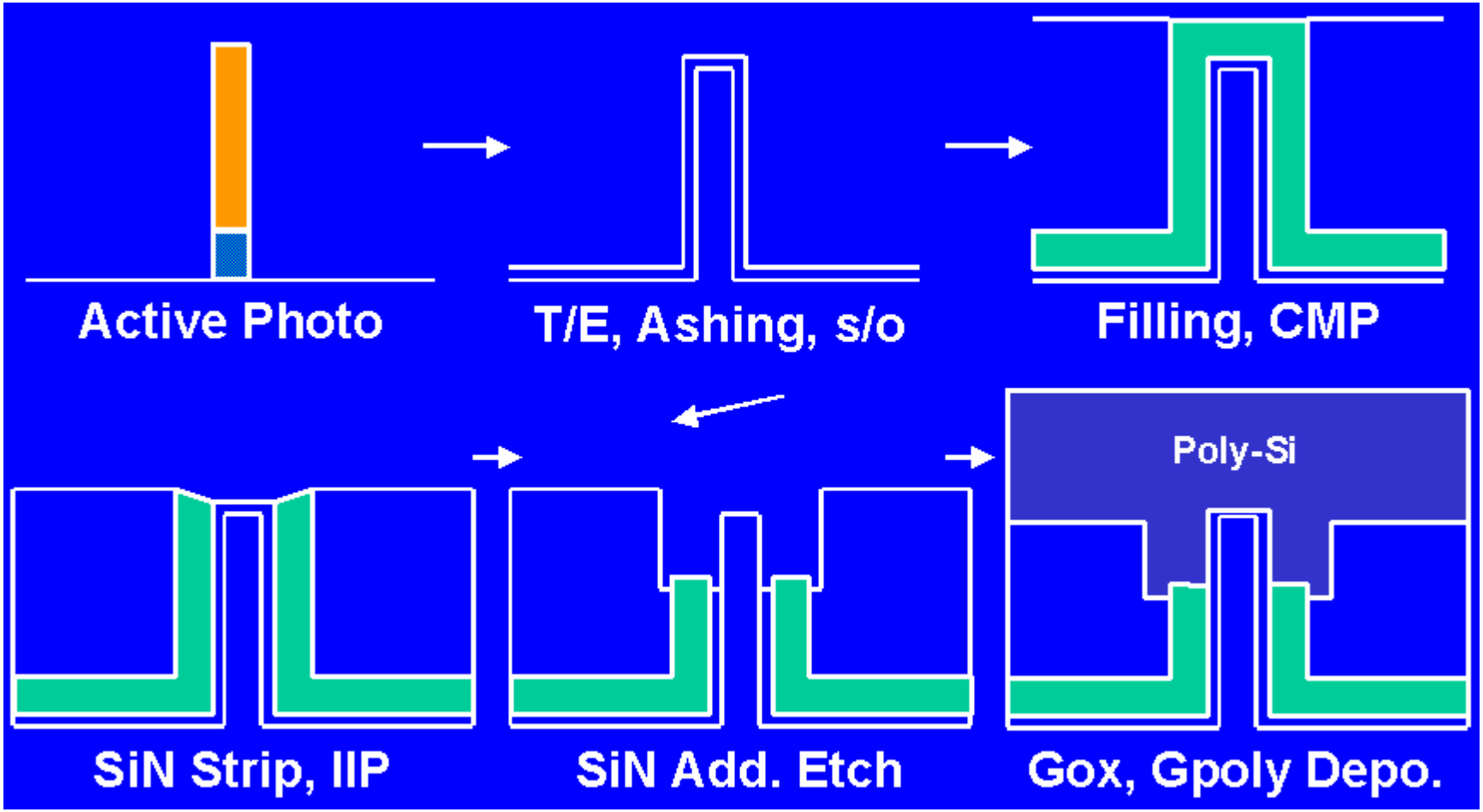




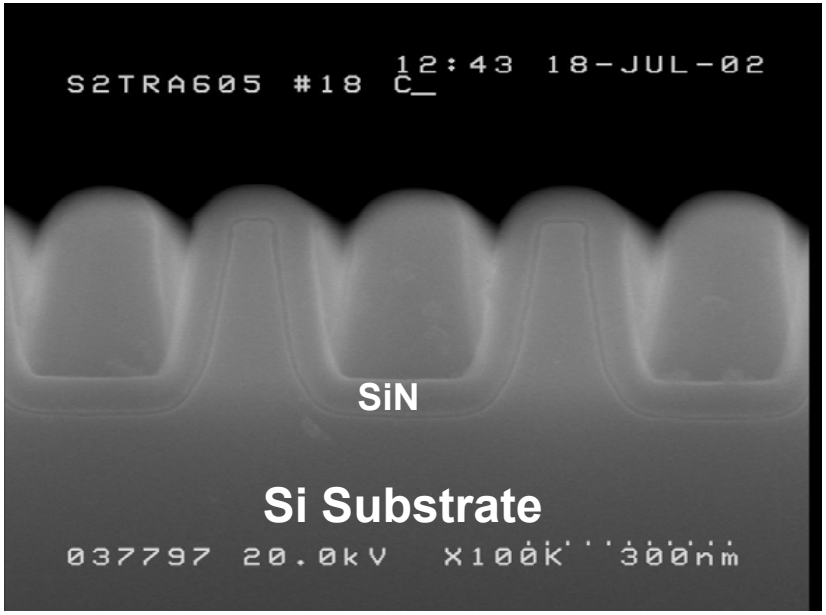
- **Clear Sidewall Open**
- **Planarization of the Top Surface of Poly-Si Gate**
  - **Easy nano-scale patterning of gate poly-Si**

* E. Yoon, J.-H. Lee, and T. park, Korea/Japan/USA/Germany patent

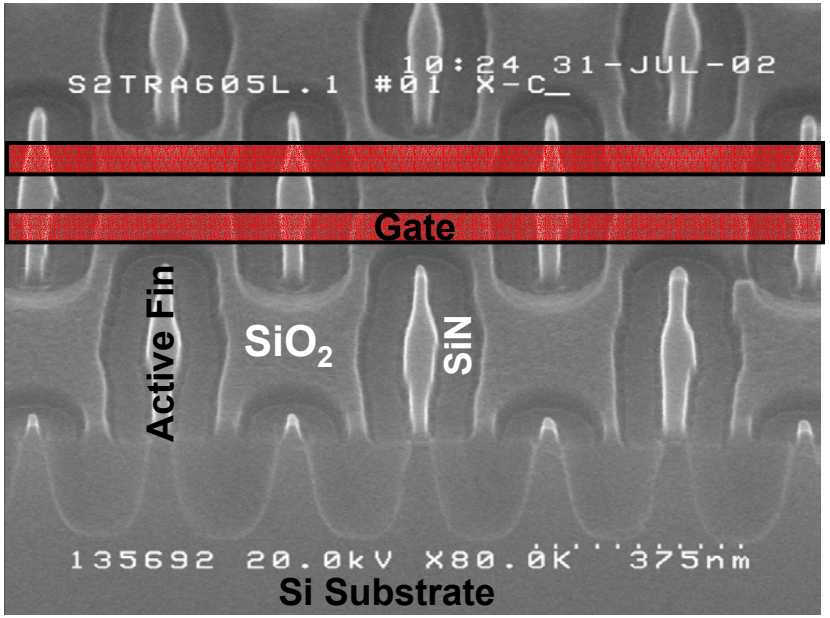
Key Process Steps of Modified Bulk FinFET



SEM Views of Key Process Steps



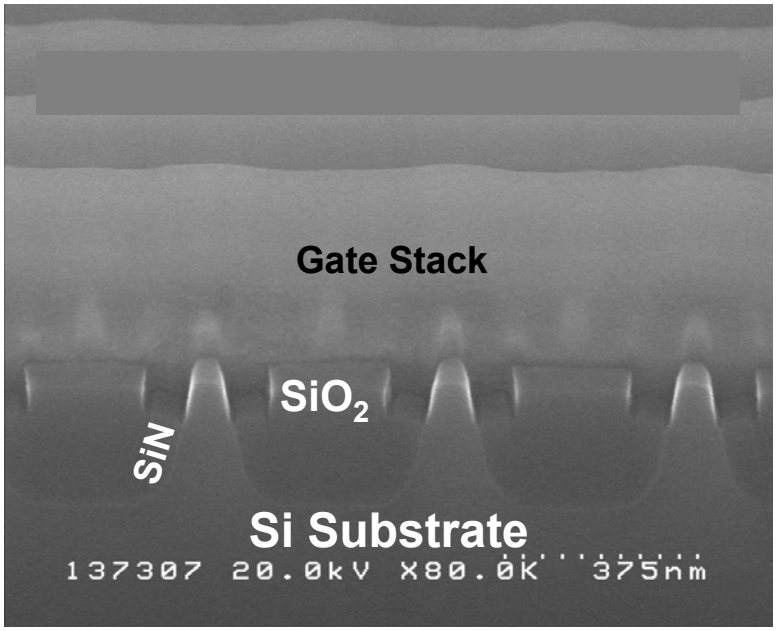
SiN Liner Deposition



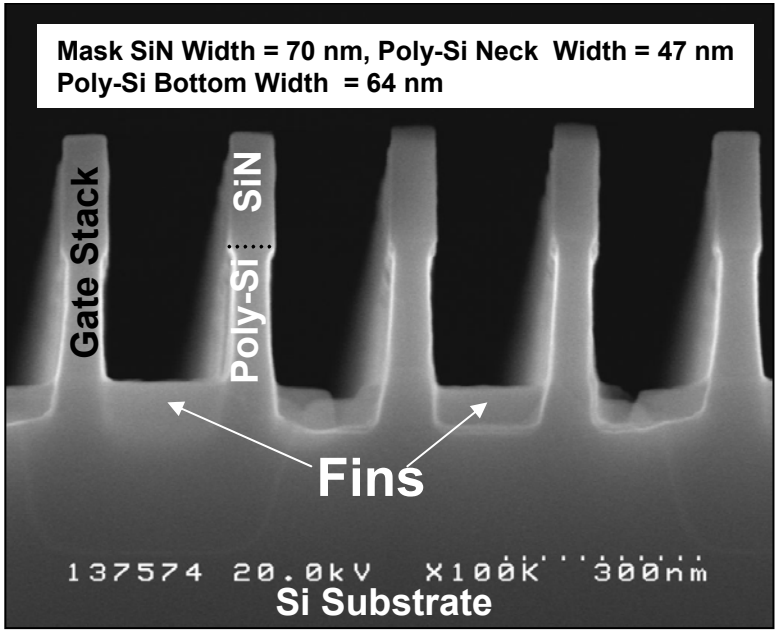
SiN Recess Etch

SEM Views of Key Process Steps

Gate Etch Profiles



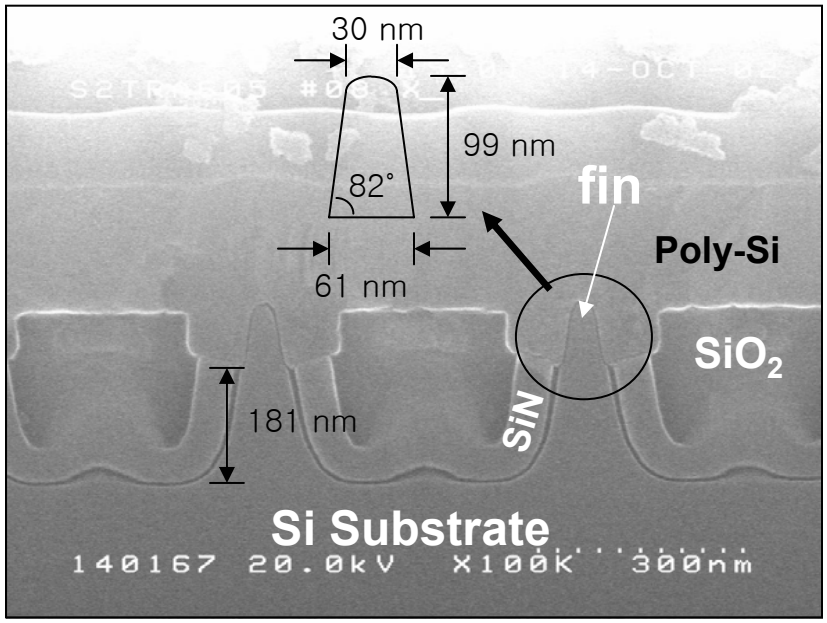
Along Gate Line



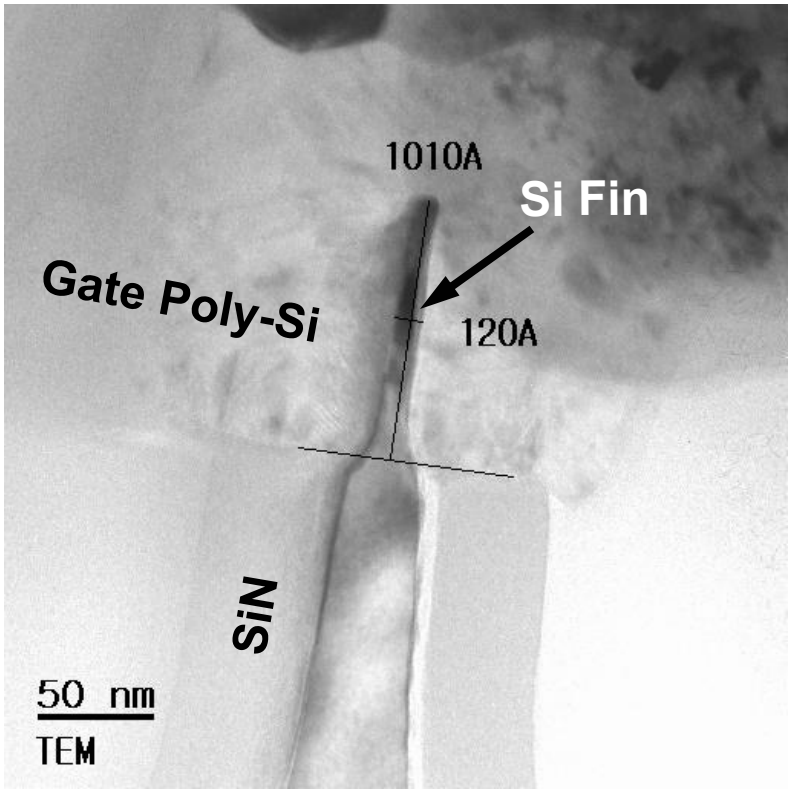
Across Gate Line

* T. Park et al., Samung/SNU/KNU, Symp. on VLSI Tech., 2003

SEM and TEM Views of Key Process Steps



Along Gate Line

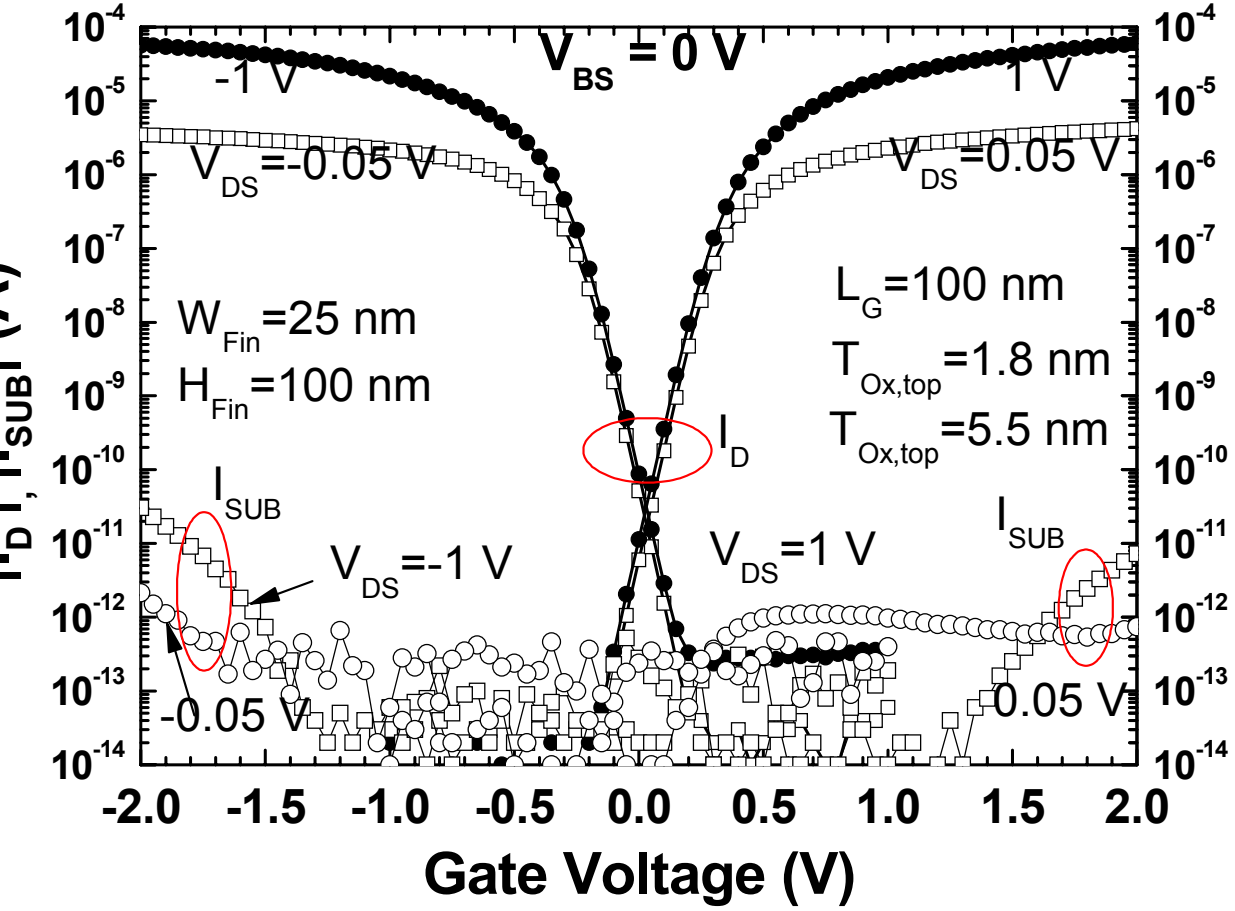


12 nm fin body

T. Park et al., Samung/SNU/KNU, IEDM., 2003

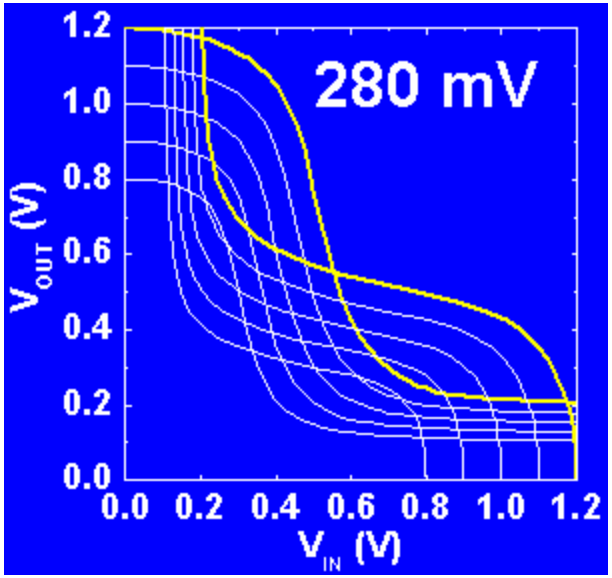
Bulk FinFET Measurement

I_D-V_{GS} plot: I_D, DIBL, SS, and I_{sub}

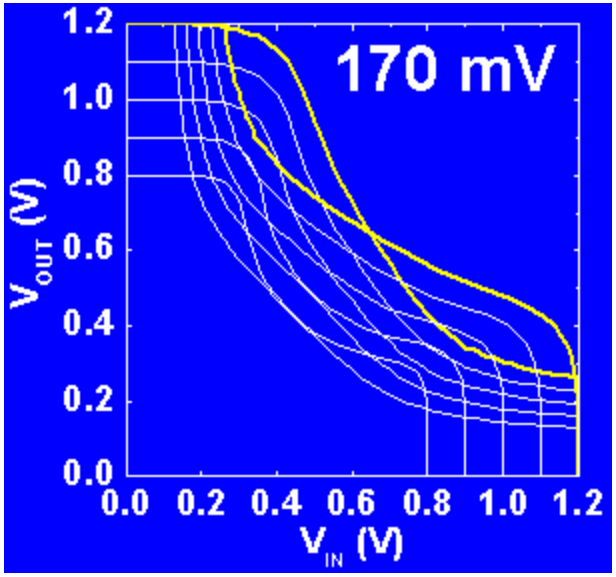


- **Measured I_D-V_{GS} of N and P type bulk FinFETs with drain bias**
  - high I_{on}(~200 μA/μm @ V_{GS}=1.5 V) compared to that of first lot devices
  - low I_{off} (<0.2 nA/μm @ V_{DS}=1.0 V)
  - I_{sub}/I_D < ~10^{-7}

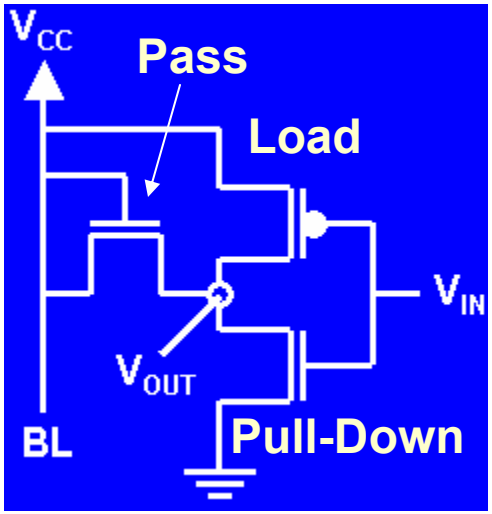
Static Noise Margin (SNM)



Bulk FinFET



Planar MOSFET



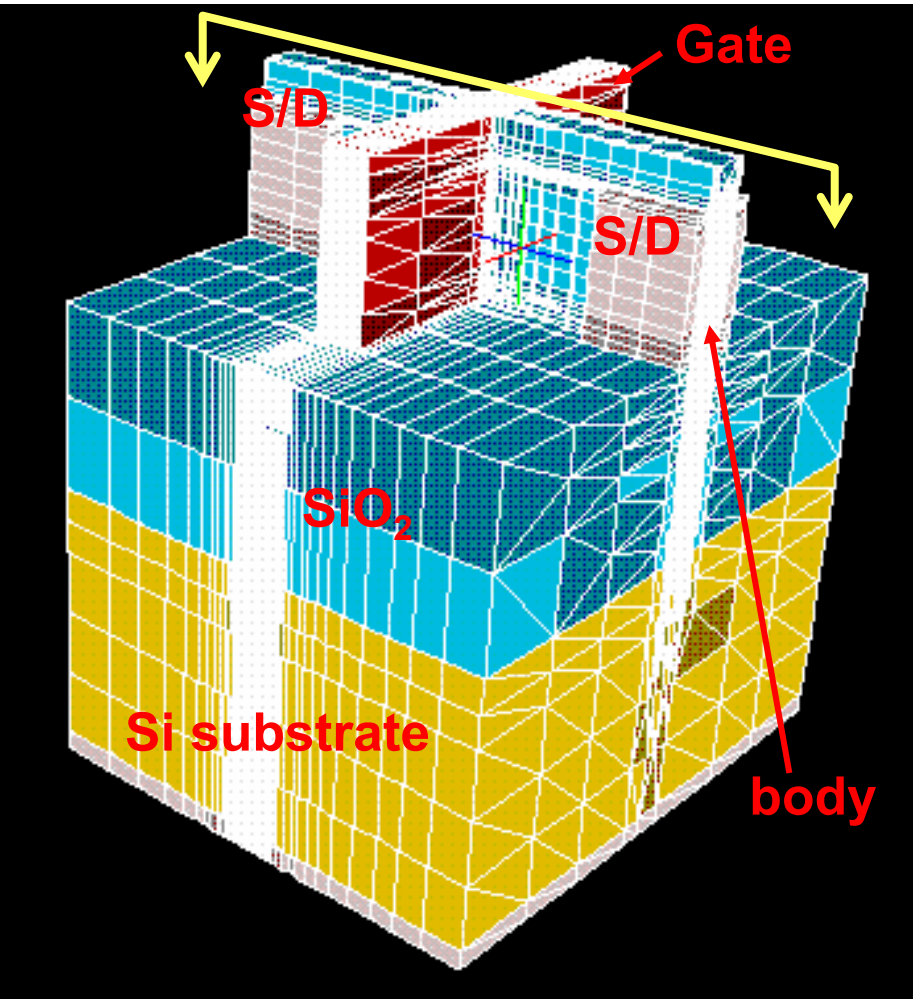
W/L

Load: 35 nm/90 nm
Pass: 35 nm/90 nm
Pull-Down: 50 nm/90 nm

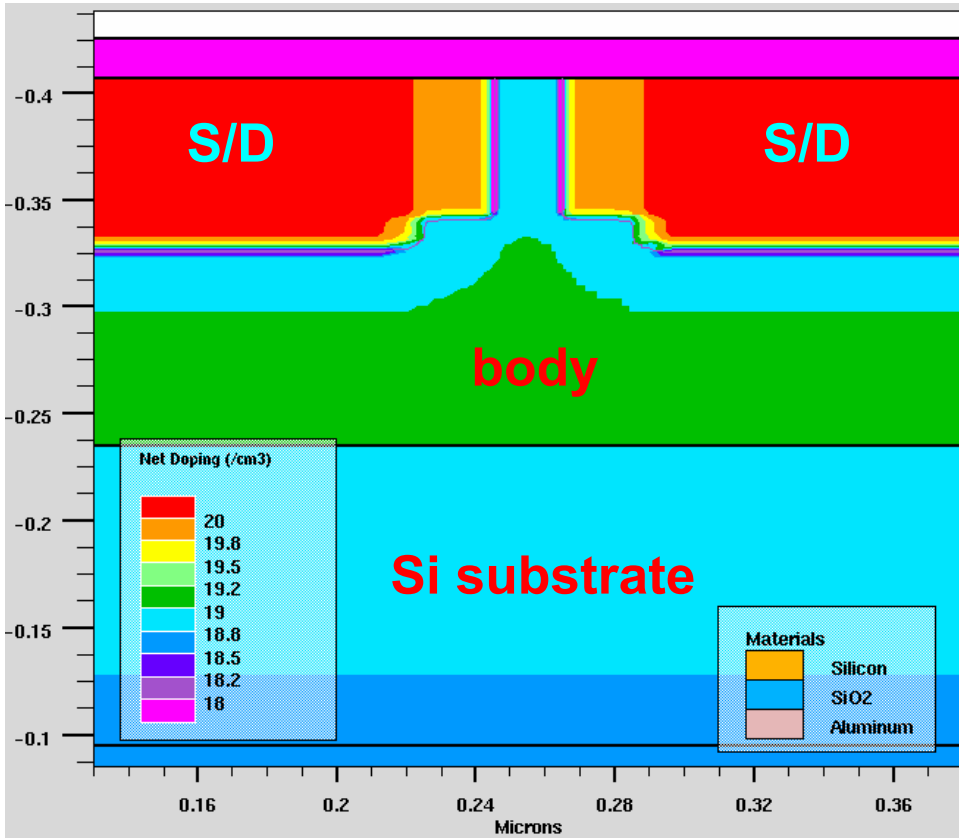
Summary

- Briefly introduced key features of double/triple-gate FinFETs
- Bulk FinFETs were compared with SOI FinFETs
  - Nearly the same device scalability
  - Better wafer quality
  - Better characteristics regarding the body connected to sub.
- Bulk FinFETs have been demonstrated experimentally
  - First nano-scale bulk FinFET realized by using spacer technology
  - Modified bulk FinFETs realized by adopting selective Si_3N_4 recess
- Good device characteristics were achieved and SNM of 280 mV was obtained from SRAM cell at V_{CC} of 1.2 V

3-D Device Structure for Simulation



L_G=25 nm T_{OX}=1.5 nm



Key Process Steps for Thinning of the Fin Body